## REMARKS

The specification has been revised to correct/clarify the grammar and to correct various self-evident errors in singular-versus-plural case, reference-symbol usage, and figure-number identification.

Additionally, typical values for voltages $V_{CPH}$, $V_{DD}$, $V_{SS}$, and $V_{SEL}$ are given at various places in the specification prior to paragraph 58, page 12. These typical values have been repeated in the first sentence of paragraph 58 in order to facilitate understanding that paragraph. In paragraph 72, page 15, "high $V_{EO}$ value" in the second sentence has been corrected to "low $V_{EO}$ value" in conformity with the immediately previous sentence that erasure-only voltage $V_{EO}$ is high at that point.

The embodiment shown in application Fig. 14 for the body-line sector decoder of body-line decoder 40 shows that the connection/disconnection of body line 70 to the $V_{SS}$ supply by way of the hard electrical path through the body-line decoder 40 is controlled solely by sector identification signals $X_{ij}$ and $Y_{ik}$. Inasmuch as sector identification signals $X_{ij}$ and $Y_{ik}$ are two of body-line selection signals $V_{BLS}$, the first sentence of paragraph 74, page 16, that "The combination of the high $V_{EI}$ value at time $t_0$ and the $V_{BLS}$ selection-signal values that result in the selection of the illustrated EPROM sector causes body line 70 for the selected sector to be electrically disconnected from the $V_{SS}$ supply by the hard electrical path through body-line decoder 40" has been corrected to state that "The $V_{BLS}$ selection-signal values that result in the selection of the illustrated EPROM sector at time $t_0$ cause body line 70 for the selected sector to be electrically disconnected from the $V_{SS}$ supply by the hard electrical path through body-line decoder 40".

The term "decoder 36" in the second sentence of paragraph 80, page 17, has been corrected to "control-line discharge circuitry 36" since the immediately previous sentence discloses that item 36 is the control-line discharge circuitry. In the course of correcting "control line 64" to "control lines 62" later in paragraph 80, the phrase "through control-line decoder 32" has been inserted between "remains electrically connected" and "to control lines 62" to make it clear that the connection of line 54 to control lines 62 continues to be made through control-line decoder 32.

Control-line discharge circuitry 36 is connected to control node $N_C$ at which erasure control voltage $V_{CE}$ is present. Circuitry 36 thus influences voltage $V_{CE}$. However, circuitry

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36 does not have any significant influence on erasure body voltage $V_{BE}$. In light of this, the references to erasure "body" voltage "$V_{BE}$" in the third sentence of paragraph 94, page 21, have been changed to erasure "control" voltage "$V_{CE}$" so that the third sentence correctly provides that "Inasmuch as the resistor(s) in the current path from line 56 through the weak-ground circuitry to the $V_{SS}$ supply could cause erasure control voltage $V_{CE}$ to vary somewhat from $V_{SS}$, the strong-ground circuitry holds voltage $V_{CE}$ close to $V_{SS}$".

The first sentence of paragraph 101, pages 22 and 23, originally recited that "The present invention is not limited to memory cells implemented with split-gate floating-gate FETs, e.g., split-gate devices having both control gates CG and select gates SG". However, the second sentence of paragraph 101 recites that "For instance, the invention encompasses memory cells implemented with split-gate floating-gate FETs having control gates CG but not select gates SG" and thus is partially inconsistent with the first sentence. To make these two sentences consistent with each other, the phrase "e.g., split-gate devices" and the comma immediately preceding "e.g." have been deleted from the first sentence so that it reads "The present invention is not limited to memory cells implemented with split-gate floating-gate FETs having both control gates CG and select gates SG". Later in paragraph 101, the word "partially" in the clause that control gate CG "extends partially over the remainder of the channel portion" in the embodiment of application Figs. 6a and 7a has been deleted since Figs. 6a and 7a show that control gate CG extends essentially fully over the remainder of the channel portion.

The third sentence of paragraph 105, page 23, original provided that "FET N5 temporarily turns off". Inasmuch as the first sentence of paragraph 105 provides that FET N5 turns off, the third sentence is redundant and has been deleted.

In paragraph 126, page 28, the disclosure that item 154 is a "NAND" gate has been corrected to provide that item 154 is a "NOR" gate since application Fig. 13 illustrates item 154 as a NOR gate. Similarly, "NOR gate 172" and "NAND gate 174" in the last sentence of paragraph 137, page 30, have been corrected to "NAND gate 172" and "NOR gate 174" inasmuch as application Fig. 14 shows that items 172 and 174 respectively are a NAND gate and a NOR gate.

Claims 1, 19, 20, 38, 40, 41, 43, and 50 have been amended. More specifically, Claim 1 has been corrected by inserting the missing term "$V_{T1}$" between "less" and "than" in

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the first subparagraph of the claim. The revisions to Claims 19, 20, 40, 41, 43, and 50 clarify the claimed subject matter. The dependency of Claim 38 has been corrected so that it depends from Claim 37.

Claims 51 - 64 have been added to claim the invention with more particularity and to cover fabrication aspects of the invention. New Claims 61 and 63 are independent claims. The remaining new claims are dependent claims. Claims 1 - 64 are now pending.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

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